IN THE CLAIMS

What is claimed is:

1. A system, comprising:

at least a first jitter buffer store having a plurality of first jitter buffer entries arranged into groups that each store data for a particular data channel, the first jitter buffer entries being accessible by first jitter buffer addresses;

at least a first valid bit store having a plurality valid buffer entries, each valid buffer entry having a plurality of bit locations that indicate the status of at least one entry from multiple groups of the first jitter buffer, the valid buffer entries being accessible by valid bit store addresses; and

an address generator that receives at least a first portion of first jitter buffer addresses to generate corresponding valid bit store addresses.

2. The system of claim 1, wherein:

the address generator generates bit mask values for valid bit store entries from at least a second portion of the first jitter buffer addresses.

3. The system of claim 1, wherein:

the address generator adds a valid bit store base address to the at least first portion of first jitter buffer addresses.

4. The system of claim 1, further including:

the at least first jitter buffer store is formed in a first memory device; and

the at least first valid bit store is formed in a second memory device.

5. The system of claim 4, wherein:

the first memory device comprises a static random access memory (SRAM).

6. The system of claim 1, wherein:

the at least first jitter buffer store includes a plurality of jitter buffer stores, each jitter buffer store including entry groups of different sizes.

7. The system of claim 6, wherein:

the plurality of jitter buffer stores includes the first jitter buffer store having entry groups that store X amount of data of a data channel, a second jitter buffer store having entry groups that store at least 2X amount of data of a data channel.

8. The system of claim 1, further including:

a time stamp counter that provides a time stamp value that is incremented; and

jitter buffer entries for data channels are periodically read from the at

least first jitter buffer according to the time stamp value.

9. The system of claim 1, further including:

a processor that reads at least a portion of the data from first jitter buffer entries and writes the at least portion of the data to a local buffer, the processor resetting the value of at least one bit in a corresponding valid buffer entry when all of a first jitter buffer entry is written to the local buffer.

10. The system of claim 9, wherein:

each first jitter buffer entry includes N portions, and the processor reads each entry N times before resetting the value of the bit in the corresponding valid buffer entry.

11. A system for storing data from multiple channels received from an asynchronous network and outputting such data to a synchronous network, comprising:

a jitter buffer arranged into a plurality of jitter buffer groups that each include M entries, where M is a real number, each jitter buffer group storing data for a different data channel;

a valid buffer having a plurality of valid buffer entry groups, each valid buffer entry including status bits corresponding to at least one of the M entries in N different jitter buffer groups; and

an address translator that translates a jitter buffer entry address for a jitter buffer entry into the valid buffer entry address having the status bit for that entry.

12. The system of claim 11, wherein:

each jitter buffer group comprises M consecutive addressable entries of a semiconductor memory device.

13. The system of claim 12, wherein:

the jitter buffer and valid buffer are formed in two different memory devices.

14. The system of claim 12, wherein:

each valid buffer entry corresponds to one particular entry in each of the N jitter buffer entry groups.

15. The system of claim 12, wherein:

the address translator includes

a base address store that stores a base address for the jitter buffer,

a separator for separating a jitter buffer address into at least a first portion and a second portion, and

an adder for adding the base address and the first portion of the jitter buffer address.

16. The system of claim 15, wherein:

one status bit in a valid buffer entry is selectable by masking the valid buffer entry according to the second portion of the jitter buffer address.

17. A method for receiving data from an asynchronous network and outputting such data to a synchronous network, comprising the steps of:

providing a jitter buffer having a plurality of entries for storing data;

providing a valid memory having a plurality of entries for storing status bits for each jitter buffer entry;

receiving data for multiple channels;

storing data segments for each channel in a corresponding group of jitter buffer entries;

setting a status bit in the valid memory entry to a valid state when data

is written to the corresponding jitter buffer entry;

reading data from jitter buffer entry; and

setting the status bit of a valid buffer entry to an invalid state when data is read from the corresponding to the jitter buffer entry.

18. The system of claim 17, wherein:

receiving data includes receiving data packets having multiplexed data.

19. The system of claim 17, wherein:

reading data segments includes reading data segments from a jitter buffer read address that includes at least a portion of a time stamp value that increments; and

setting a status bit in a valid buffer entry includes swizzling the read address to generate the corresponding jitter buffer entry.

20. The system of claim 17, wherein:

storing data segments includes writing data segments to a jitter buffer write address that includes at least a portion of a time stamp value that increments; and

setting a status bit in a valid buffer entry includes swizzling the write address to generate the corresponding jitter buffer entry.